Docket No.: W1878.0169/P169
(PATENT)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:
Tomoaki Aihara

Application No.: 09/832,666 | Confirmation No.: 1818

Filed: April 11, 2001 | Art Unit: 2829

For: METHOD AND APPARATUS FOR INSPECTING SEMICONDUCTOR DEVICE | Examiner: J. Nguyen

SUBMISSION OF TRANSLATION OF JAPANESE PATENT APPLICATION

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

Applicant's attorney hereby submits a Verification of Translation and translation of Japanese Patent Application No. 2000-114045 to perfect the claim for priority.

In the Advisory Action dated December 2, 2003, the Examiner referred to U.S. Patent No. 6,642,707. Applicant respectfully points out that the '707 patent is not prior art. The present application claims priority to Japanese Patent Application No. 2000-114045, filed April 14, 2002. The '707 patent was filed on September 13, 2002. As such, the present application predates the '707 patent.

If the Examiner believes an interview would be of assistance, the Examiner is welcome to contact the undersigned at the number listed below.

Dated: March 17, 2004

Respectfully submitted,

By_____

Ian R. Blum
Registration No.: 42,336
DICKSTEIN SHAPIRO MORIN &
OSHINSKY LLP
1177 Avenue of the Americas
41st Floor
New York, New York 10036-2714
(212) 835-1400
Attorney for Applicant

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Japanese Application of

Tomoaki AIHARA

Japanese Patent Application No. 2000-114045

Japanese Patent Filing Date: April 14, 2000

for: "Method and Apparatus for Inspecting Semiconductor Device"

VERIFICATION OF TRANSLATION

Honorable Commissioner of Patents and Trademarks

Washington, D.C. 20231

Sir:

Junichi TANAKA residing at 4-18-24, Maeharacho, Koganei-shi, Tokyo, Japan, declares:

(1) that he knows well both the Japanese and English languages;

(2) that he translated the above-identified U.S. Application from Japanese to English;

(3) that the attached English translation is a true and correct translation of the above-identified Japanese Application to the best of his knowledge and belief; and

(4) that all statements made of his own knowledge are true and that all statements made on information and belief are believed to be true, and further that these statements are made with the knowledge that willful false statements and the like are punishable by fine or imprisonment, or both, under 18 USC 1001, and that such false statements may jeopardize the validity of the application or any patent issuing thereof.

February 26, 2004

Date

Junichi Tanaka

Junichi TANAKA

[Document Name] Patent Application

[Docket Number] 74410393

[Filing Date] April 14, 2000

[To] Commissioner, Patent Office

[International Classification] G01R 31/28
H01L 21/66

[Inventor]

[Address or Domicile] c/o NEC Corporation, 7-1, Shiba 5-chome, Minato-ku, Tokyo

[Name] Tomoaki AIHARA

[Applicant for Patent]

[Identification Number] 000004237

[Name or Appellation] NEC Corporation

[Agent]

[Identification Number] 100088328

[Patent Attorney]

[Name or Appellation] Nobuyuki KANEDA

[Telephone Number] 03-3585-1882

[Agent]

[Identification Number] 100106297

[Patent Attorney]

[Name or Appellation] Katsuhiro ITO

[Agent]

[Identification Number] 100106138

[Patent Attorney]

[Name or Appellation] Masayuki ISHIBASHI

[Indication of Official Fees]

[Advance Deposit Record Number] 089681

[Amount paid] 21000

[List of Materials submitted]

[Material Name]	Specification	1
[Material Name]	Drawings	1
[Material Name]	Abstract	1
[Number of General Power of Attorney]		9710078

[Proof] Requested

[Name of document] SPECIFICATION

[Title of the invention] Method and Apparatus for Inspecting Semiconductor Device

[Scope of claim]

[Claim 1] An inspection method of simultaneously inspecting a plurality of semiconductor devices each having a terminal for an input signal, comprising the steps of:

preparing with a driver for outputting a signal to be used for inspection;

connecting an output terminal of said driver to a branching point;

connecting each of the terminals of the semiconductor devices and the branching point through a current limiting element and a capacitor connected in parallel to said current limiting element; and

outputting a signal from said driver toward said branching point.

[Claim 2] An inspection method for simultaneously inspecting a plurality of semiconductor devices each having a first terminal and a second terminal for inputting respective input signals, comprising the steps of:

preparing with a first and second drivers for outputting corresponding signals to be used for inspection;

connecting an output terminal of said first driver to a branching point;

connecting each of the first terminals of the semiconductor devices and the branching point through a current limiting element and a capacitor connected in parallel to said current limiting element;

connecting output terminal of said second driver and the second terminal of the semiconductor device one to one each other; and

outputting a signal from said first driver toward said branching point and outputting another signal from said second drivers to said second terminal of the semiconductor device.

[Claim 3] An inspection method according to claim 1 or 2, wherein a resistor is used as said current limiting element.

[Claim 4] An inspection method according to claim 3, wherein resistance value of said resistor is set equal to or higher than 10 Ω.

[Claim 5] An inspection method according to any one of claims 1 to 4, wherein capacitance value of said capacitor is set equal to or higher than input capacitance value of the terminal to be connected.

[Claim 6] An inspection method according to any one of claims 1 to 5, wherein DC input resistance value of each of the terminals is equal to or higher than 0.1 MΩ.

[Claim 7] An inspection method according to any one of claims 1 to 6, wherein the semiconductor devices operate in synchronism with an external clock, and frequency of the external clock is equal to or higher than 10 MHz.

[Claim 8]. An inspection apparatus for simultaneously inspecting a plurality of semiconductor devices each having a terminal for an input signal, comprising:

a driver for outputting a signal to be used for inspection;

a branching point to which an output terminal of said driver is connected;

a current limiting element interposed between each of the terminals of the semiconductor devices and said branching point; and

a capacitor connected in parallel to each of the current limiting elements.

[Claim 9] An inspection apparatus for simultaneously inspecting a plurality of semiconductor devices each having a first terminal and a second terminal for receiving respective input signals, comprising of:

a first driver and a second driver for outputting corresponding signals to be used for inspection;

a branching point to which an output terminal of said first driver is

connected;

a current limiting element interposed between each of the first terminals of the semiconductor devices and said branching point; and

a capacitor connected in parallel to said current limiting element;

wherein output terminals of said second drivers and the second terminals of the semiconductors are connected respectively one to one directly.

[Claim 10] An inspection apparatus according to claim 8 or 9, wherein said branching point, the current limiting elements and the capacitors are provided within a probe card or a test board for connecting semiconductor device to be inspected to a tester.

[Claim 11] An inspection apparatus according to any one of claims 8 to 10, wherein said current limiting element is a resistor.

[Claim 12] An inspection apparatus according to claim 11, wherein resistance value of said resistor is equal to or higher than 10 Ω.

[Claim 13] An inspection apparatus according to any one of claims 8 to 12, wherein capacitance value of said capacitor is equal to or higher than input capacitance value of the terminal to be connected.

[Claim 14] An inspection apparatus according to any one of claims 8 to 13, wherein DC input resistance value of the terminal is equal to or higher than 0.1MΩ.

[Claim 15] An inspection apparatus according to any one of claims 8 to14, wherein said semiconductor operates synchronously with a clock supplied from external source and its frequency is equal or higher than 10 MHz to said second terminal.

[Detailed explanation of the invention]

[0001]

[Technical field to which the invention pertains]

The present invention relates to a method of and an apparatus for inspecting semiconductor devices such as semiconductor integrated circuits and semiconductor memory devices, and more particularly to an inspection method and an inspection apparatus for inspecting semiconductor devices having capability to inspect the number of semiconductor devices to be inspected simultaneously is increased.

[0002]

[Prior art]

A semiconductor device of the inspection object may be referred to also as DUT (Device Under Test). When a semiconductor device is inspected upon manufacture or delivery, usually a semiconductor tester and the DUT are connected to each other through a probe card or a test board. Then, a predetermined inspection signal is applied to each pad or each pin for an input signal of the semiconductor device under the inspection, and a signal at each pad or each pin for an output signal of the semiconductor device is detected.

[0003]

In the field of semiconductor devices, a terminology is sometimes used in different manners depending upon whether a semiconductor device is not packaged as yet or is packaged already in such a manner that, for the semiconductor device before packaged, a representation "to connect to a pad using a probe card " is used, but for the semiconductor device after packaged, another representation "to connect to a pin using a test board" is used. In the following description, however, pads and pins of semiconductor devices are generally referred to as terminals. Also the probe card which is used for connecting a semiconductor device to be inspected to a tester includes a test board.

[0004]

In inspection of a semiconductor device, it is requested to minimize the inspection time. Therefore, it has been attempted to inspect a plurality of semiconductor devices simultaneously. FIG. 6 shows a basic configuration for inspecting a plurality of semiconductor devices simultaneously using a single tester.

[0005]

Tester 61 for inspecting semiconductor devices in accordance with a test program includes a plurality of drivers 62 each for applying a predetermined signal to a terminal 65 for an input signal of semiconductor device 64 to be inspected. Each of semiconductor devices 64 has a plurality of terminals 65 each for an input signal. Tester 61 and semiconductor devices 64 are connected to each other through probe card 63. One driver 62 in tester 61 corresponds to one terminal 65, therefore, a number of drivers 62 greater than the total number of input terminals 65 of the semiconductor devices 64 to be inspected are prepared.

[0006]

Consequently, in the configuration described above, a number of drivers equal to the total number of terminals for an input signal of semiconductor devices to be inspected simultaneously must be prepared in the tester. Therefore, the configuration described has a problem in that the tester has a large-scale configuration. Further, the number of the drivers that are provided in the tester limits the number of semiconductor devices that can be inspected simultaneously. Therefore, the configuration has another problem in that the number of simultaneously inspected semiconductor devices cannot be increased very much.

[0007]

It is generally considered that semiconductor devices that are inspected

simultaneously are of the same type. Thus, Japanese Patent Laid-Open No. 11-231022 (JP, 11231022, A) discloses an apparatus wherein a signal from a driver of a tester is branched in a probe card and supplied in parallel to a plurality of semiconductor devices to be inspected simultaneously as seen from FIG. 7. A wiring scheme by which a signal from a driver is branched and supplied in parallel to a plurality of semiconductor devices is called common drive wiring, and a driver used in such common drive wiring is called common driver.

[0008]

In the configuration shown in FIG. 7, three terminals 65a to 65c, 65d to 65f for an input signal are provided for each of a plurality of semiconductor devices 64a, 64b. The output of driver 62a from the drivers in tester 61 is connected one to one to terminal 65a of semiconductor device 64a, and the output of driver 62d is connected one to one to terminal 65d of another semiconductor device 64b. However, the output of driver 62b is branched at branching point 66a in probe card 63 and supplied to terminal 65b of semiconductor device 64a and terminal 65e of semiconductor device 64b. Similarly, the output of driver 62c is branched at branching point 66b in probe card 63 and supplied to terminal 65c of semiconductor device 64a and terminal 65f of semiconductor device 64b. Since the output of each of drivers 62b, 62c is branched and connected to a plurality of terminals for an input signal, drivers 62b, 62c are common drivers.

[0009]

Such a configuration as described above includes a driver that takes charge of a plurality of terminals and therefore allows a greater number of semiconductor devices to be inspected with a small number of drivers used.

[0010]

This configuration, however, has a problem in that, if one of semiconductor devices inspected simultaneously has a defect such as leak or a

short-circuit at an input terminal, inspection of the remaining normal semiconductor devices is disabled. Where the input terminal of a semiconductor device to be inspected has a MOS (metal-oxide-semiconductor) transistor configuration or a CMOS (complementary MOS) configuration, it is considered that the input resistance of the input terminal is equal to or higher than 0.5 MΩ, typically equal to or higher than approximately 3 MΩ. Therefore, the drivers in a tester are so configured that the current driving capacity thereof may conform to the input resistance. Then, if leak of 100 Ω or less when converted into an input resistance for DC, for example, occurs with one of a plurality of input terminals to which a signal branched from a driver is applied, a normal signal voltage is not applied to the normal input terminals either. This disables inspection of a normal semiconductor device as well.

[0011]

This is described in connection with the example shown in FIG. 7. It is assumed here that semiconductor device 64a is a non-defective unit and semiconductor device 64b is a defective unit in that leak occurs with input terminal 65e thereof. Terminal 65e with which leak occurs and terminal 65b of semiconductor device 64a of a non-defective unit are connected in parallel with input terminal 65e to driver 62b. Therefore, when terminals 65b, 65e are driven by driver 62b, because of the leak at terminal 65e, a regular signal voltage is not applied to normal terminal 65b either, and also semiconductor device 64a of a non-defective unit cannot be inspected normally.

[0012]

As a countermeasure to solve the problem described above where a signal from a driver is branched and applied to a plurality of input terminals, it is attempted to insert a resistor of approximately several hundreds ohms between a branching point and each input terminal after a signal from a driver is branched in

a probe card as seen in FIG. 8. The configuration shown in FIG. 8 is a modification to the configuration shown in FIG. 7 in that resistors 67 of approximately several hundreds ohms (600 Ω, for example) are inserted between branching point 66a and terminal 65b, between branching point 66a and terminal 65e, between branching point 66b and terminal 65c, and between branching point 66b and terminal 65f.

[0013]

Although this configuration is effective for inspection of a semiconductor device whose clock frequency is comparatively low such as approximately 10 MHz or less, it cannot be used for inspection of a semiconductor device whose clock frequency is higher than 30 MHz. The reason is that, since the input capacitance of each input terminal of a semiconductor device to be inspected is typically 5 pF and provides a time constant of approximately 3 ns together with the inserted register (typically having a resistance of approximately 600 Ω), the application timing of the signal to the input terminals is delayed as much and the waveform of the signal applied thereto is distorted. Further, the dispersion in input capacitance disperses the delay time itself for each terminal.

[0014]

Also with the circuit configuration shown in FIG. 7 or FIG. 8, a signal to which a delay or distortion of the waveform is extremely unfavorable like a reference clock which determines an operation timing of a semiconductor device is supplied to a clock input terminal without being branched from a driver. If some delay occurs with a certain data input terminal as described above, the signal is not latched correctly at the data input terminal when the latch operation is synchronized to the clock signal supplied to the clock input signal. Further, extreme distortion of a signal renders operation of the semiconductor device unstable as well.

[0015]

FIG. 9 is a diagram illustrating a disadvantage where a waveform suffers from some delay or distortion. Waveform b is a waveform to be latched at a rising edge of waveform a, and it is assumed here that waveform b falls prior to a rising edge of waveform a. Also it is assumed that a resistor is interposed between the driver that outputs waveform b and a terminal of a semiconductor device to be inspected to which waveform b is inputted. Furthermore, it is assumed that the threshold voltage of the latch is just equal to one half power supply voltage Vcc, and consequently, it is discriminated that the input voltage has the "H" (high) level when it is equal to or higher than Vcc/2, but the input voltage has the "L" (low) level when it is lower than Vcc/2. The solid line curve of waveform b indicates a waveform when no resister is interposed (i.e., waveform at the output point of the driver) and a broken line indicates a waveform at the input terminal of the semiconductor device when the resistor is inserted as seen in FIG. 8. As seen from FIG. 9, where a resistor is connected to the driver which outputs waveform b, waveform b still remains at the "H" level at the point of time of the rising edge of waveform a, and therefore, the semiconductor device cannot latch a signal correctly.

[0016]

In recent years, the clock frequency of a semiconductor memory device, for example, has raised from 66 MHz to 100 MHz and further to 250 MHz, and utilization also of a higher clock frequency is proceeding steadily. Also the bus frequency of a microprocessor has been and is raised similarly. Thus, the delay caused by an inserted resistor restricts the number of simultaneously inspected semiconductor devices of the type described and significantly disturbs augmentation in efficiency of the inspection.

[0017]

[Problem to be solved by the invention]

With the conventional inspection methods described above, as the operation speed of a semiconductor device increases, it becomes more difficult to increase the number of semiconductor devices which can be inspected simultaneously without increasing the required number of drivers in a tester while a defect of one of semiconductor devices inspected simultaneously is prevented from having a bad influence on the other normal semiconductor devices.

[0018]

It is an object of the present invention to provide an inspection method for a semiconductor device by which an increased number of semiconductor devices can be inspected simultaneously without increasing the number of drivers in a tester even where the semiconductor devices of the inspection object are of the type which operates at a high speed.

[0019]

[Means for solving the problem]

In the present invention, when a common drive wiring line is used to branch a signal from a driver so that the signal is supplied in parallel to a plurality of input terminals through respective resisters, a capacitor is connected in parallel to each resistor. This simple circuit configuration wherein a capacitor is connected in this manner can suppress delay or distortion of a signal applied to the input terminal even where a resistor is inserted in the common drive wiring line. As a result, a large number of semiconductor devices whose clock frequency is higher than 30 MHz can be inspected simultaneously.

[0020]

The resistor is used to prevent a defect like a leak defect, which may incidentally occur with one of semiconductor devices connected to the common drive wiring line, from having an influence on the other semiconductor devices,

and acts to suppress over current which may flow due to such leak defect. Accordingly, in the present invention, the resistor may be replaced by any current limiting element such as a thermistor having a positive temperature coefficient or a constant current circuit element which utilizes a threshold value-current characteristic of a junction field effect transistor (JFET), for example. Also a resistor is included in the criterion of the current limiting element in the present invention.

[0021]

Where a resistor is used as the current limiting element, the resistance value of the resistor is determined suitably in accordance with the DC input resistance value or the input capacitance value of the input terminal of the semiconductor device to be inspected. However, where the input terminals of the semiconductor device have a MOS transistor configuration or a CMOS configuration, for example, and have a DC input resistance value equal to or higher than 3 MΩ, the resistance value of the resistor is set within the range from 50 Ω to 1 kΩ, more preferably within the range from 50 Ω to 200 Ω.

[0022]

Meanwhile, preferably the capacitance value of the capacitor connected in parallel to the resistor is equal to or higher than the input capacitance of each input terminal of the semiconductor device to be inspected. More strictly, the capacitance value of the capacitor preferably is equal to or higher than an input capacitance value (a designed value or a value on a catalogue, for example) of the input terminal to be connected thereto when the terminal is normal, and more preferably is equal to or higher than 1.5 times the input capacitance value. Since the input terminals of a MOS transistor configuration or a CMOS configuration usually have an input capacitance value of 3 to 5 pF although they have somewhat different input capacitance values before and after the

semiconductor device is packaged, the capacitance value of the capacitor connected in parallel to the resistor preferably is equal to or higher than 5 pF, more preferably is equal to or higher than 7 pF, and further more preferably is equal to or higher than 10 pF. However, if the capacitance value is excessively high, then the volume of the capacitor may be so large that it may possibly be difficult to accommodate a required number of capacitors in a probe card or a test board. Further, where leak current at an input terminal of a semiconductor device of the inspection object is very large due to a defect, this unfavorably provides a capacitive load to the driver of the tester. The upper limit to the capacitance value of the capacitor preferably is equal to or lower than 10 times the input capacitance, for example, and more preferably is equal to or lower than 50 pF.

[0023]

In the present invention, it is possible to use an element having a variable resistance value as the resistor or current limiting element. Further, it is possible to use an element having a variable capacitance value as the capacitor that is connected in parallel to the resistor or current limiting element. Use of such a variable resistor and/or a variable capacitor allows selection of an optimum resistance value and/or an optimum capacitance value in accordance with an electric characteristic of the input terminals of the semiconductor device to be inspected, a clock frequency or the driving capacity of the driver.

[0024]

In the present invention, the number of branches from one driver in the tester by the common drive wiring line is not limited to 2 but is adjusted suitably in accordance with the number of semiconductor devices to be inspected simultaneously or with some other parameter. The number of branches may be three, four or more, for example.

[0025]

The semiconductor device to which the present invention can be applied suitably is a semiconductor device such as a semiconductor memory device, a microprocessor or an ASIC (application specific integrate DC circuit) whose driving clock or reference clock has a frequency equal to or higher than 10 MHz, typically equal to or higher than 50 MHz. A semiconductor memory device, a microprocessor or an ASIC whose reference clock has one of frequencies of 66 MHz, 100 MHz and 133 MHz, for example, is applicable to this. The driving clock or the reference clock here signifies a clock signal that is supplied as a reference to a timing for fetching or outputting of a signal to the semiconductor device. According to the present invention, a plurality of semiconductor devices can be inspected simultaneously through the common drive wiring line even where the clock frequency for the semiconductor devices is 250 MHz, for example.

[0026]

Furthermore, the present invention is suitably applied also to a semiconductor device for which it is required that the rise time or the fall time of a signal is equal to or shorter than 10 ns, typically equal to or shorter than 5 ns. The time required for an input voltage to rise from its 10 % value to its 90 % value is called rise time and the time required for an input voltage to fall from its 90 % value to its 10 % value is called fall time in accordance with a common custom in the pertaining field.

[0027]

[Mode for carrying out the invention]

A preferable mode for carrying out the invention is explained referring to attached drawings. Fig. 1 shows a configuration of an inspection apparatus for semiconductor devices according to the mode for carrying out the present

invention.

[0028]

It is assumed that, in FIG. 1 which shows a configuration of a semiconductor device inspection apparatus of a preferred embodiment according to the present invention, tester 11 is used to inspect two semiconductor devices 14a, 14b simultaneously, for the convenience of description. Each of semiconductor devices 14a, 14b includes three inputting terminals 15a to 15c, 15d to 15f. Tester 11 includes a plurality of drivers 12a, 12b, 12c, 12d, ..., and signals from the drivers are applied to semiconductor devices 14a, 14b for inspection through probe card 13.

[0029]

The output of driver 12a is connected one to one to terminal 15a of semiconductor device 14a, and also the output of driver 12d is connected to terminal 15d of semiconductor device 14b. Therefore, the wiring lines for them are not common drive wiring lines.

[0030]

On the other hand, the output of driver 12b is branched to two branches at branching point 16a in probe card 13, and one of the branches is connected to inputting terminal 15b of semiconductor device 14a while the other branch is connected to inputting terminal 15e of semiconductor device 14b. Resistor 17 is interposed between branching point 16a and terminal 15b. Further, capacitor 18 is connected in parallel to resistor 17. Similarly, resistor 17 is interposed between branching point 16a and terminal 15e, a capacitor 18 is connected in parallel to resistor 17. In other words, the output of driver 12b is connected to a common drive wiring line. Resistors 17 and capacitors 18 are provided in probe card 13.

[0031]

Also the output of driver 12c is branched to two branches at branching point 16b in probe card 13 and is connected to a common drive wiring line similarly to the output of driver 12b. In particular, resistor 17 is interposed between branching point 16b and terminal 15c, and capacitor 18 is connected in parallel to resistor 17. Resistor 17 is interposed between branching point 16b and terminal 15f as well, and capacitor 18 is connected in parallel to resistor 17.

[0032]

Each of inputting terminals 15a to 15f has a DC input resistance value of 3 MΩ, for example, and has an input capacitance of 3 pF. In this instance, a resistor of 100 Ω, for example, is used for each resistor 17, and a capacitor of a capacitance of 10 pF is used for each capacitor 18.

[0033]

In the example shown in FIG. 1, the common drive wiring is applied to terminals 15b, 15c, 15e, 15f from among the input terminals of semiconductor devices 14a, 14b, but is not applied to the remaining terminals 15a, 15d.

[0034]

Those terminals to which the common drive wiring is applied and those terminals to which the common drive wiring is not applied are present in a mixed state in this manner, and they may be applied separately in the following manner. Where, the semiconductor device for the inspection object is a semiconductor memory device such as a DRAM (Dynamic Random Access Memory), for example, a clock signal is used as a reference to operation of the memory device (and accordingly provides a reference to the timing upon inspection). Further, the clock signal is frequently prescribed strictly in terms of the duty ratio and the waveform. Accordingly, generally the common drive wiring is not applied to the clock signal. On the other hand, preferably the common drive wiring is applied to an address line, data line, a CAS (column address strobe) signal and a RAS

(row address strobe) signal those are fetched in synchronism with the clock signal so that the required number of drivers in the tester may be decreased. Such criteria as described here can be applied also to the case that an object of the inspection of semiconductor device is a microprocessor.

[0035]

FIGS. 2 (a) to (e) are diagrams for comparison between waveforms at specific portions of the configuration of the present embodiment and waveforms at the same specific portions of the conventional configuration shown in FIG. 8. FIG. 2(a) shows standard signals, i.e., the output waveforms of the drivers. FIGS. 2(b) and 2(c) show waveforms at input terminals 15a to 15f of the configuration shown in FIG. 1 when the signals illustrated in FIG. 2(a) are outputted from the drivers. Meanwhile, FIGS. 2(d) and 2(e) show waveforms at input terminals 65a to 65f of the conventional configuration shown in FIG. 8, that is, the configuration wherein only resisters are inserted in a common drive wiring line when the signals illustrated in FIG. 2(a) are outputted from the drivers.

[0036]

In this case, the input capacitance of each input terminals of the semiconductor device to be inspected is 5 pF; the input resistance of each input terminal is 3 MΩ; the resistance value of each resistor inserted in the common drive wiring lines is 300 Ω; and the capacitance of each capacitor connected in parallel to the resistor is 50 pF.

[0037]

As seen in FIG. 2(a), waveform A outputted from driver 12a (62a) is a pulse with the pulse width of 15 ns; waveform B outputted from driver 12b (62b) is a pulse which rises earlier by 1 ns than a rising edge of waveform A; and waveform C outputted from driver 12c (62c) is a pulse which falls earlier by 1 ns than a rising edge of waveform A. Accordingly, if waveform B and waveform C

are latched at the rising edge of waveform A, then they become signals having level of "H" and "L", respectively.

[0038]

Here, if only a resistor is inserted, the signals of waveform B and waveform C are distorted as seen in FIGS. 2(d) and 2(e), respectively, therefore, the waveforms cannot be latched correctly. On the other hand, where a capacitor is connected in parallel to the resistor in accordance with the present embodiment, the logic levels of waveform B and waveform C can be latched correctly although the potential level drops a little at rising and falling edges of waveform B and waveform C, respectively, as seen in FIGS. 2(b) and 2(c). Consequently, with the method of the present embodiment, semiconductor devices can be inspected correctly.

[0039]

While an embodiment of the present invention has been described, the present invention is not limited to the specific embodiment described above. The number of branches from a driver in the common drive wiring, for example, is not limited to 2 but may be increased to 3 or more. FIG. 3 shows an example wherein the number of branches of a common drive wiring line is 3

[0040].

The configuration shown in FIG. 3 is a modification of the configuration shown in FIG. 1, semiconductor device 14c having input terminals 15g to 15i is additionally provided as a semiconductor device for the inspection object. The output of driver 12e in tester 11 is connected one to one to terminal 15g of semiconductor device 14c while the output of driver 12b is connected to terminal 15h, and the output of driver 12c is connected to terminal 15i. Naturally, resistor 17 is interposed between the branching point and each terminal in probe card 13, and capacitor 18 is connected in parallel to the resistor 17.

[0041]

While an example having three branches is just described, also any common driving wiring line that has four or more branches is naturally included in the scope of the present invention.

[0042]

Further, in the present invention, various elements can be used as a current limiting element. FIG. 4 shows an example wherein thermistor 21 is used in place of each resistor in the configuration show in FIG. 1. Since a leak defect of an inputting terminal is a DC defect, use of a thermistor having a positive temperature coefficient can raise the effective resistance value as viewed from the driver to the terminal with which the leak defect occurs and can lower the effective resistance value as viewed from the driver to a normal terminal. Consequently, the influence of a terminal having leak on the other normal terminals can be suppressed to the minimum, and the resistance value of the resistor inserted for each normal terminal can be suppressed low thereby to minimize the delay amount of a signal at each normal terminal.

[0043]

In the configuration described above, a fixed resistor is interposed between a branching point and a terminal of a semiconductor device to be inspected, and a fixed capacitor is connected in parallel to the fixed resistor. However, a variable resistor and a variable capacitor (variable capacity) may be used instead, respectively. FIG. 5 shows an example which is a modification of the configuration shown in FIG. 1 in that variable resistor 22 is used in place of each resistor and variable capacitor 23 is used in place of each capacitor. Where a variable resistor and a variable capacitor are used in this manner, an optimum resistance value and/or capacitance value can be selected in accordance with the electric characteristic of an input terminal of a semiconductor

device to be inspected, the clock frequency, or the driving capacity of the drivers.

[0044]

[Effect of the invention]

As described above, the inspection apparatus for simultaneously inspecting a plurality of semiconductors according to the present invention comprises a resistor having a capacitor connected in parallel to the resistor is inserted to the common drive wiring lines respectively, so that the delay or distortion of a signal applied to an input terminal of a semiconductor device to be inspected can be suppressed with a simple circuit configuration without being influenced by defective semiconductor device connected simultaneously. Consequently, the invention has brought a great advantage that a large number of semiconductor devices whose clock frequency is as high as 10 MHz or more such as semiconductor devices whose clock frequency is 66 MHz or 133 MHz, for example, can be inspected simultaneously.

[Brief explanation of drawing]

[Fig. 1]

FIG. 1 is a circuit diagram showing a configuration of a semiconductor device inspection apparatus of a preferred embodiment of the present invention.

[Fig. 2]

FIG. 2 (a) shows a waveform which is outputted from driver, (b) and (c) show waveforms of waves which applied to input terminals of the semiconductors for inspection shown in Fig. 1, (d) and (e) show waveforms of waves applied to the terminals of the semiconductor devices for inspection shown in Fig 8.

[Fig. 3]

Fig. 3 shows a circuit diagram of configuration of another embodiment of inspection apparatus for inspecting semiconductor devices simultaneously according to the present invention.

[Fig. 4]

Fig. 4 shows a configuration of the still another embodiment of inspection apparatus for inspecting semiconductor devices simultaneously according to the present invention.

[Fig. 5]

Fig. 5 is a circuit diagram showing configuration of the further another embodiment of the inspection apparatus for inspecting semiconductor device according to the present invention.

[Fig. 6]

Fig. 6 is a circuit diagram illustrating an example of conventional inspection method of inspecting semiconductor device.

[Fig. 7]

FIG. 7 is a circuit diagram illustrating another example of conventional inspection method of inspecting a semiconductor device.

[Fig. 8]

FIG. 8 is a circuit diagram illustrating a further example of conventional inspection method of inspecting a semiconductor device.

[Fig. 9]

FIG. 9 is a diagram showing waveforms in the configuration shown in FIG. 8.

[Description of reference numerals]

11, 61 tester

12a to 12e, 62,a to 62d driver

13, 63, probe card

14a to 14c, 64,64a, 64b semiconductor device

15a to 15i, 65, 65a to 65f terminal

16a, 16b, 66a, 66b blanching point

17, 67, resistor

18 capacitor

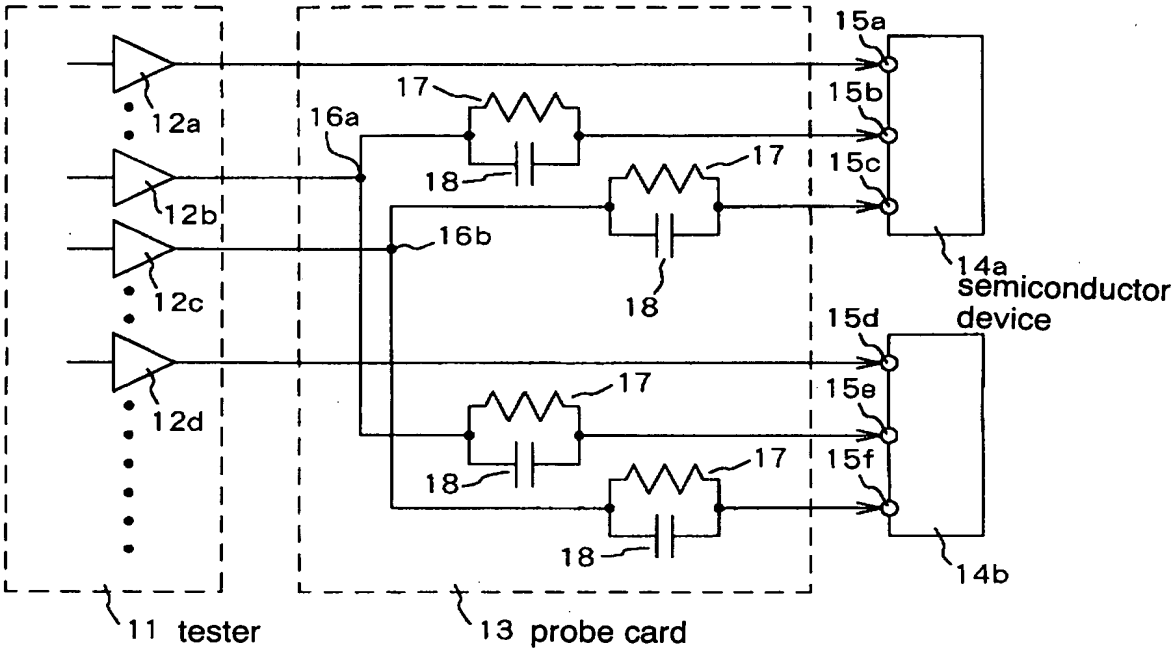
21 thermistor

22 variable resistor

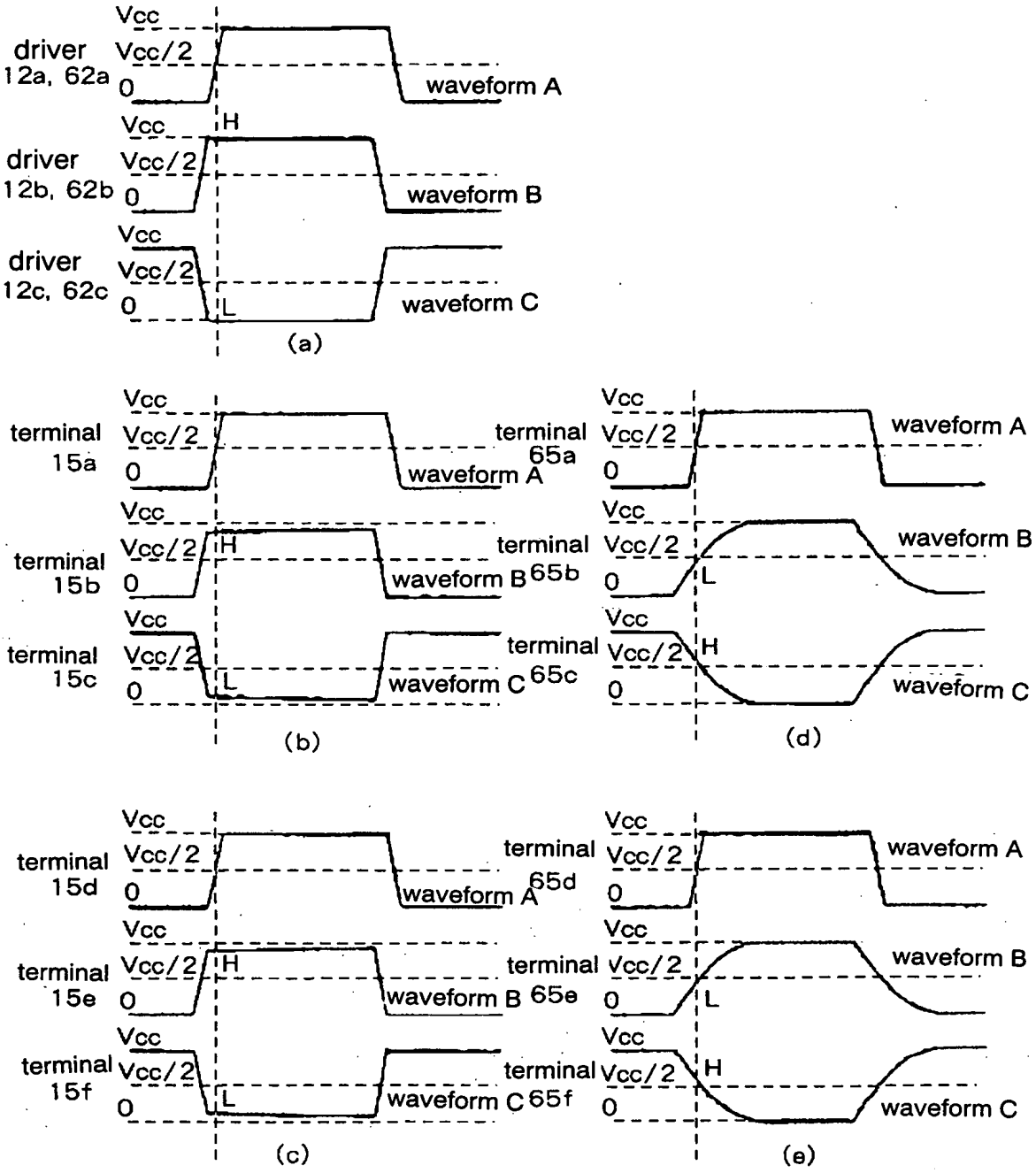
23 variable capacitor

[Name of Document] Drawings

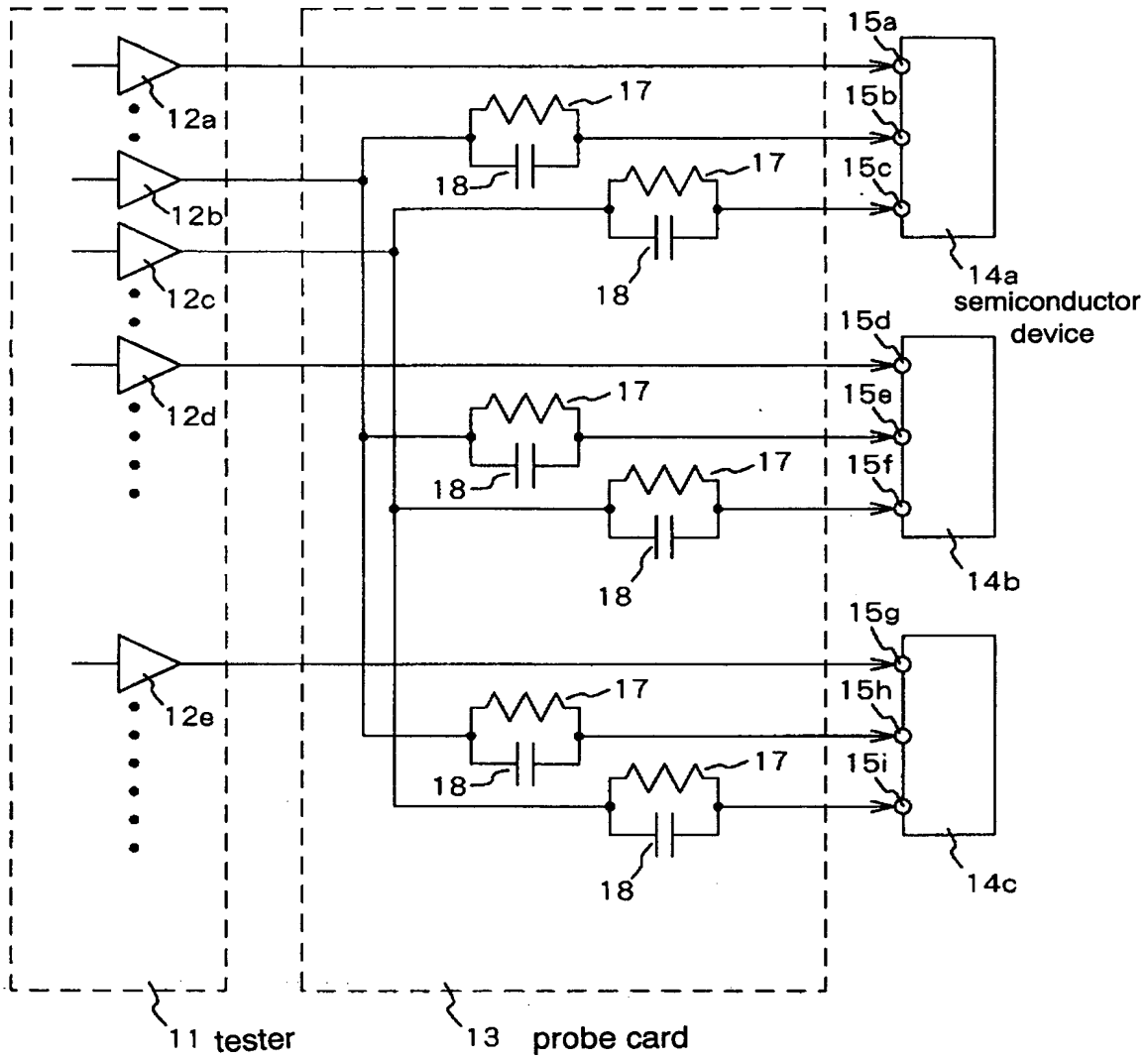
[Fig. 1]



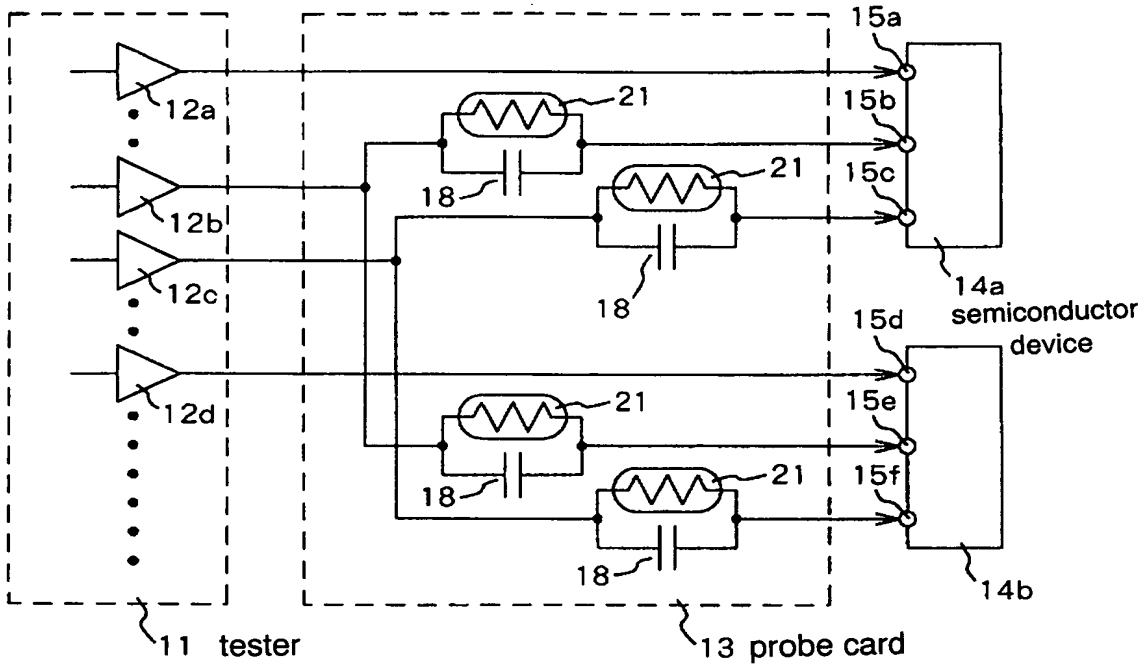
[Fig. 2]



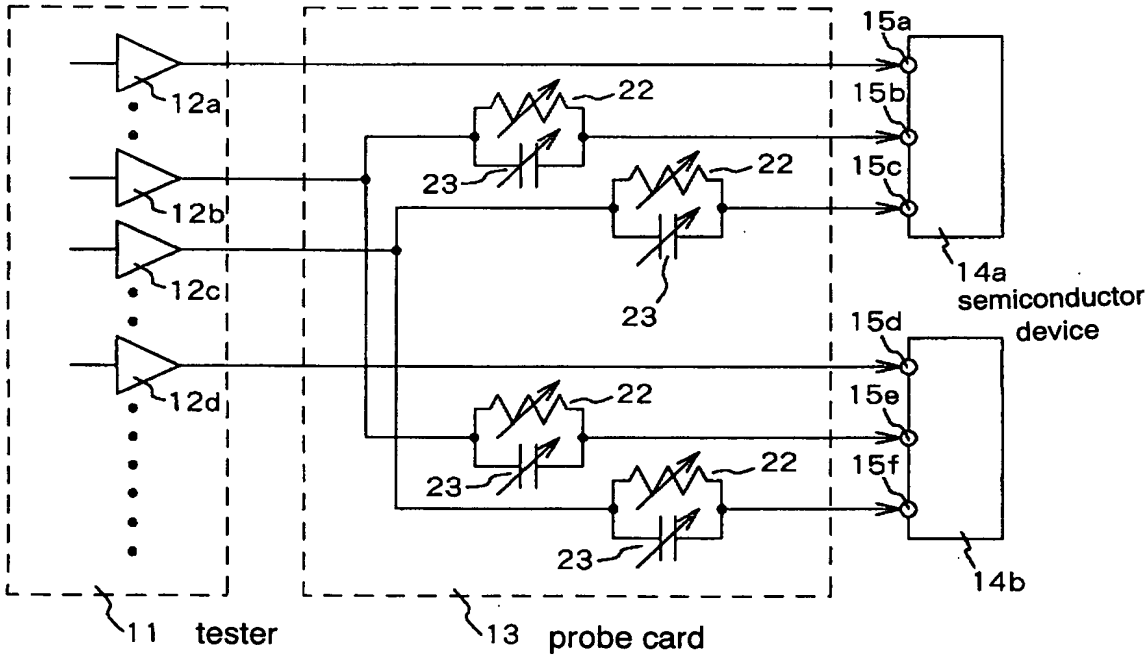
[Fig. 3]



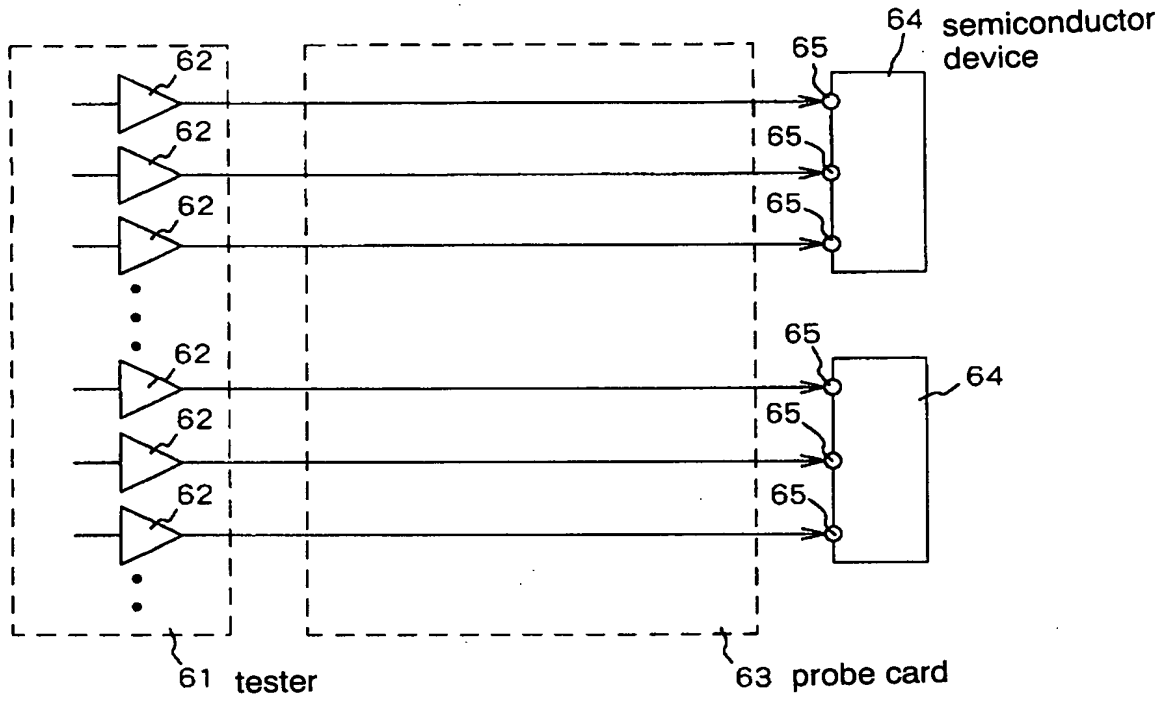
[Fig. 4]



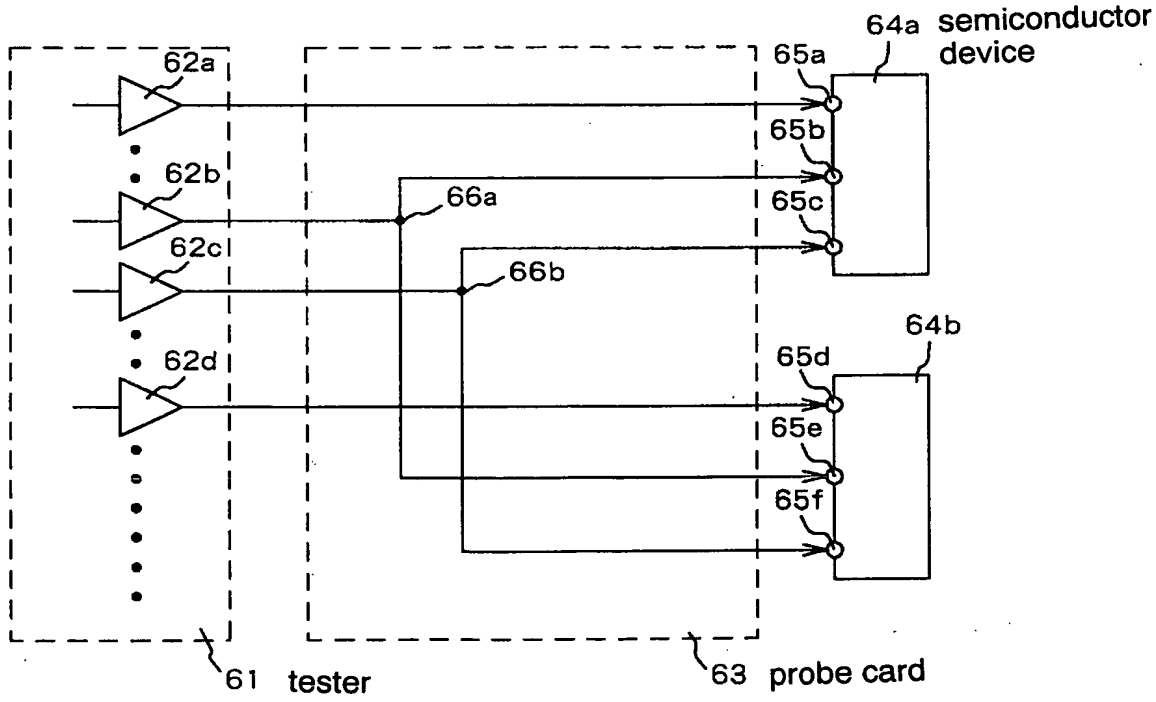
[Fig. 5]



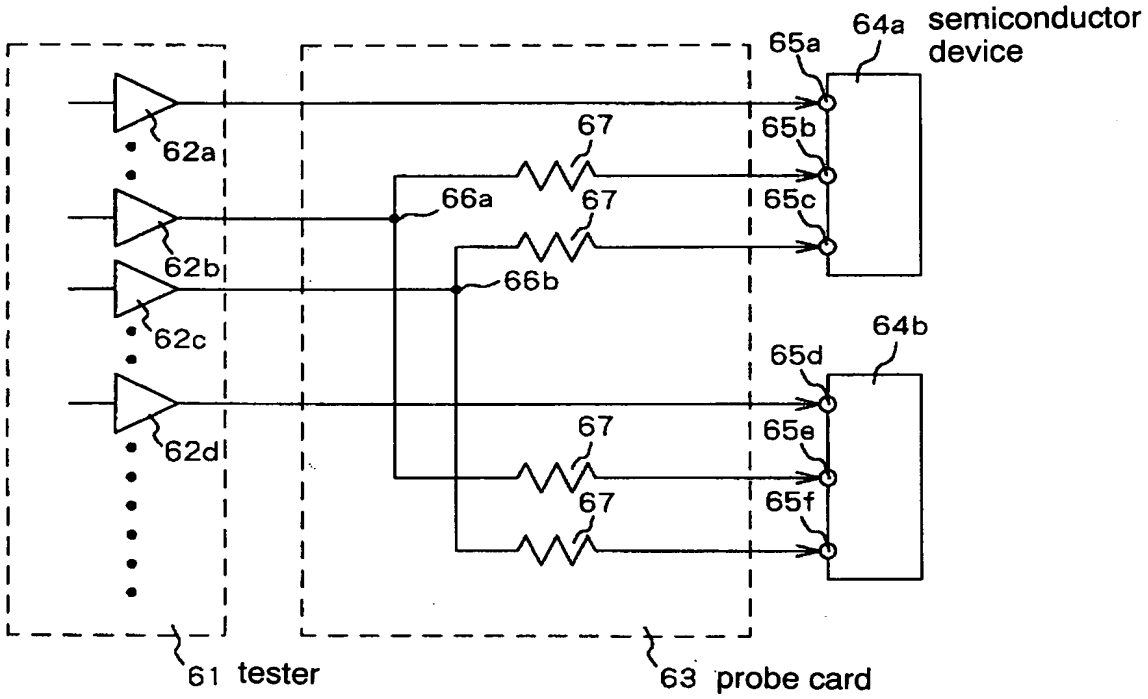
[Fig. 6]



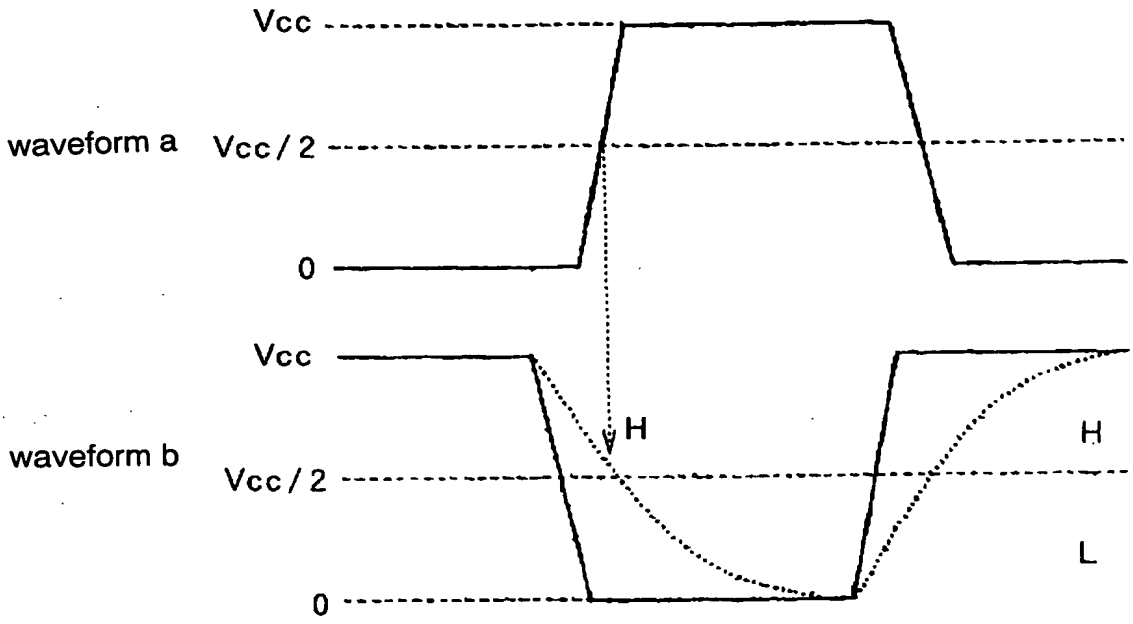
[Fig. 7]



[Fig. 8]



[Fig. 9]



[Name of document] ABSTRACT

[Abstract]

[Problem] An inspection method and apparatus for inspecting semiconductor devices, whose clock frequency is very high, having ability to increase the number of semiconductor devices to be inspected simultaneously can be increased in large amount without increasing driver is proposed.

[Means for solving the problem] In the common drive wiring for blanching a test signal outputted from the corresponding driver 12b (12c) in tester 11 into input terminals 15b, 15e (15c, 15f) of a plurality of semiconductor devices 14a, 14b via blanching point, a circuit consists of a resistor 17 and a capacitor 18 connected in parallel to the resistor 17 is inserted in the common drive wiring line between a blanching point 16a (16b) provided in probe card 13 and each input terminals 15b, 15e respectively. Capacitance of the capacitor 18 is determined to a value larger than the input capacitance of respective input terminals.

[Chosen drawing] Fig. 1